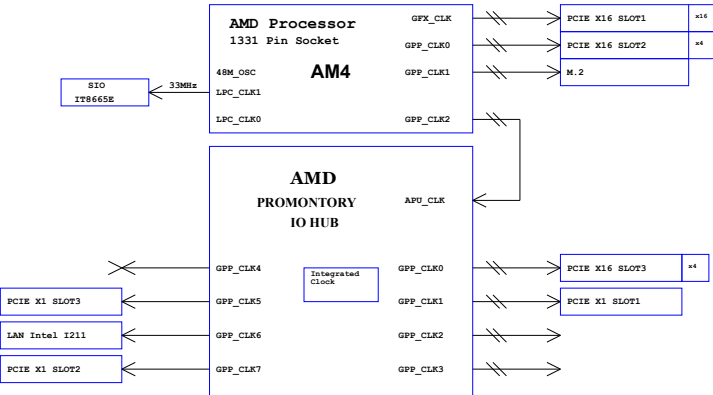




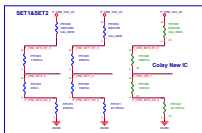
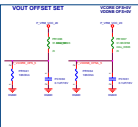
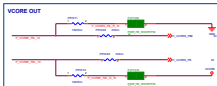
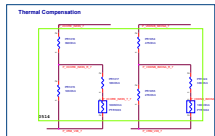
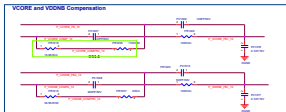
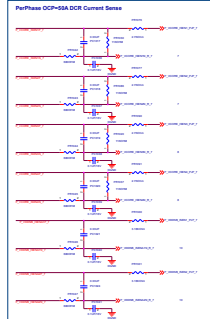
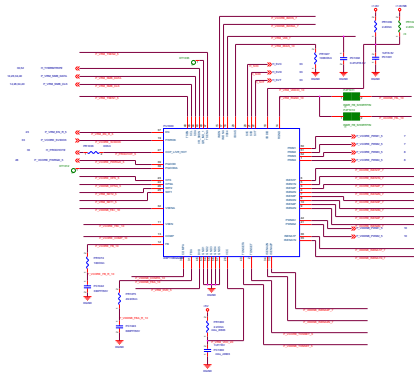


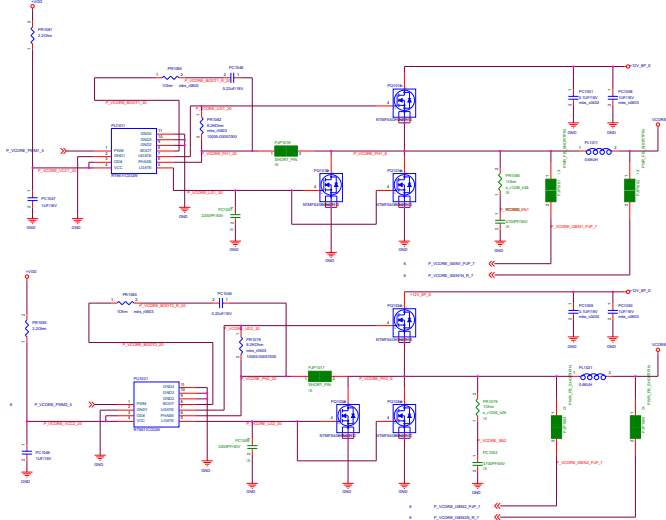
# ICG : Integrated Clock Gen.





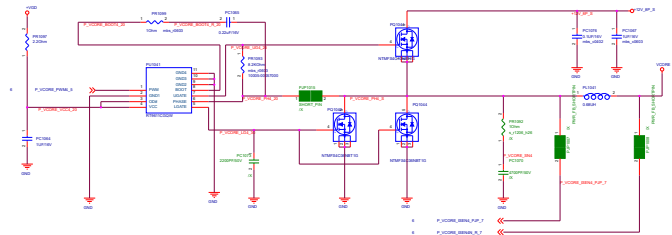
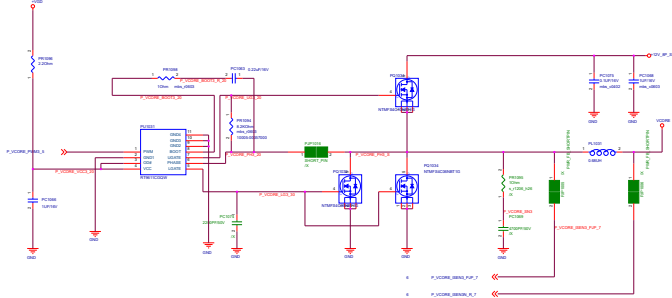
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<b>ASUS</b>		Title : DRIVER	
ASUS Computer Inc.		Engineer:	
Rev	Project Name		Rev
A1	15Q4 FM2R2 ASP1106 4-3PH 1P2P-1P2P 100		1.00
Date	2014.05.18.2014		



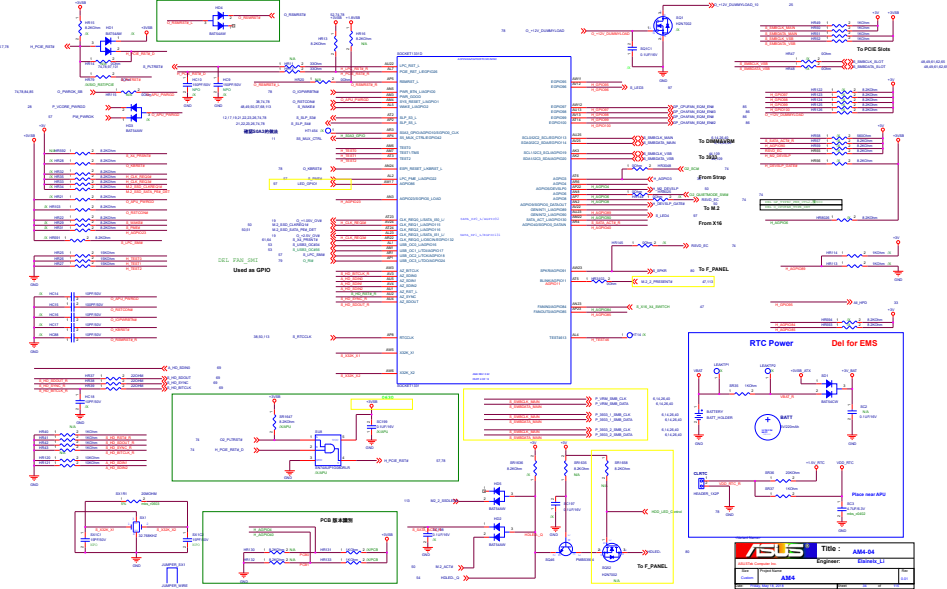
©2014 Taiwan

	<b>Title :</b> <b>VDDSOC Controller</b>
---	---

<b>ASUSTek Computer Inc.</b>	<b>Engineer:</b>
------------------------------	------------------

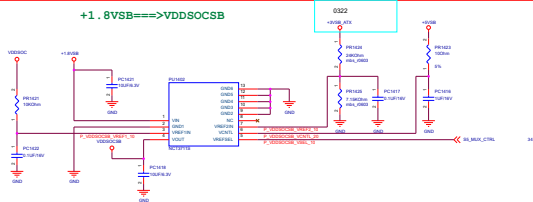
Size	Project Name	Rev
A3	<b>16Q3 AM4 1405I 6-4PH 1P1P-1P1P 100</b>	2.00





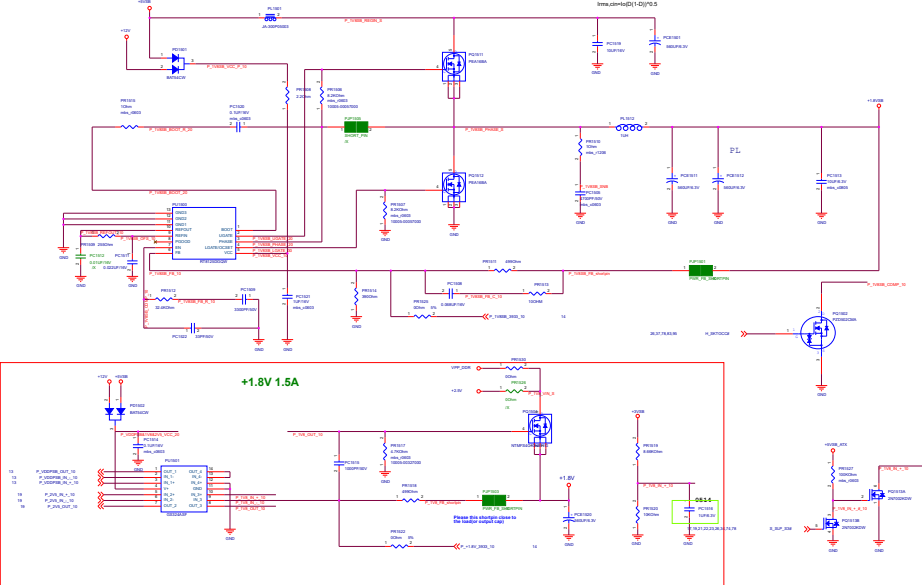


+1.8VSB==>VDDSOCSB



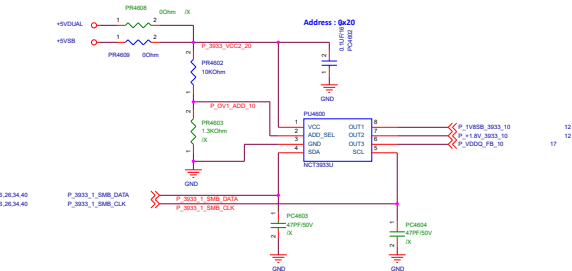
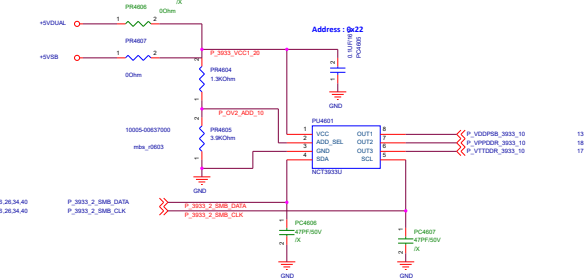
<Variant Name>

<b>ASUS</b>		Title : VDDSOCSB	
ASUS Inc. Computer Inc.		Engineer:	
Size	Project Name	Rev	Rev
A3	AM4	1.00	
Date	Friday, May 18, 2018	Sheet	11 of 11



Sheet: 1/1





<Variant Name>

<b>ASUS</b>		Title : NA	
ASUSTek Computer Inc.		Engineer:	
Size	Project Name		Rev
A4	AM4		1.00
Date:	Friday, May 18, 2018		Sheet 14 of 115



**Title :** NA

ASUSTek Computer Inc.

**Engineer:**

Size

Project Name

Rev

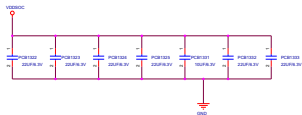
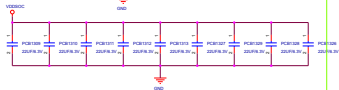
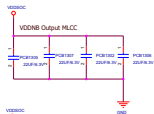
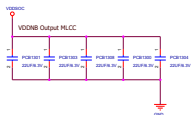
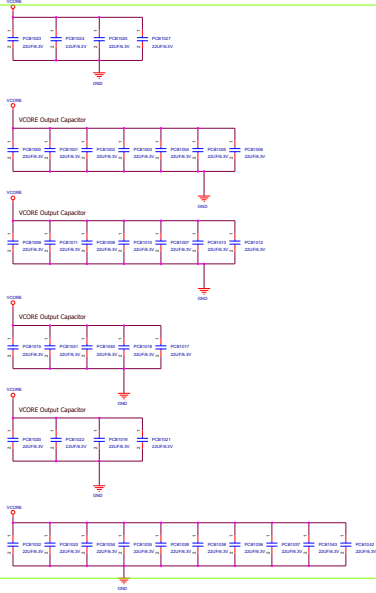
A3

**AM4**

1.00

Date: Friday, May 18, 2018

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0514

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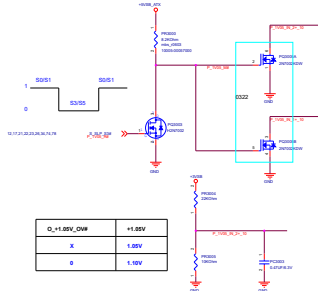
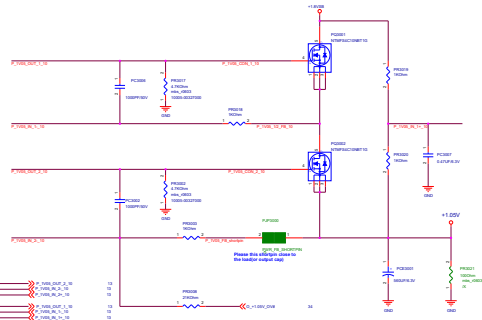




FWDC=4.7V 5.1V 5.9V

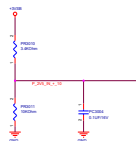
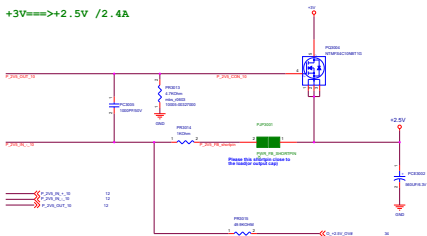


1.8VSB==>+1.05V /3A



O <sub>2</sub> +1.05V_OVR	+1.05V
X	1.05V
0	1.10V

+3V==>+2.5V /2.4A



O <sub>2</sub> +2.5V_OVR	+2.5V
X	2.55V
0	2.55V

Original Name:



**Title :**

ASUSTek Computer Inc.

**Engineer:**

**Elainex\_Li**

Size

**A3**

Project Name

**AM4**

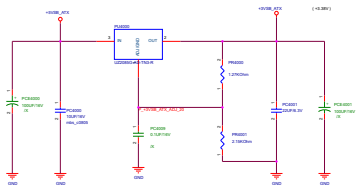
Rev

**R1.00**

Date: **Friday, May 18, 2018**

Sheet **4** of **115**

# +5VSB\_ATX ==>+3VSB\_ATX\_LDO



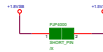
I<sub>o</sub>:1.5A

# +3VSB\_ATX => +1.05VSB 50mA



Power Component place near each other!

# +1.8VSB==>+1.5VSB 0.75A

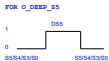
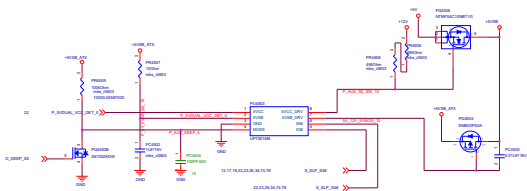


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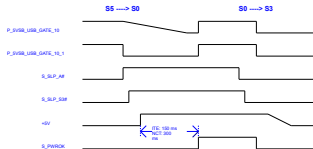
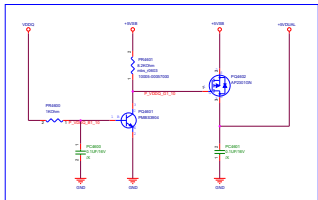
NOTE:which power rail power to audio ic should be confirmed by EE.

- 1.Vin and Vout keep more than 30mils away
- 2.Input cap and Output cap can't use same GND.
- 3.P\_SVSS\_GATE\_30 is away from Vin more than 15mils, from Vout more than 30mils.

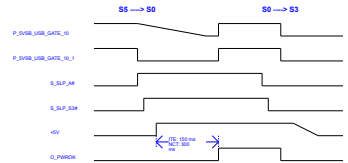
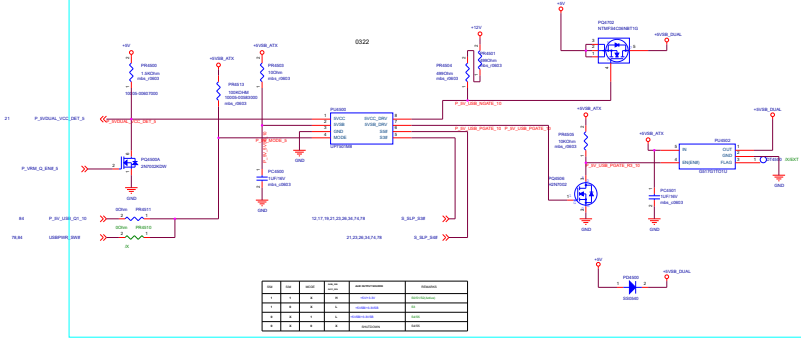
If OVP protection circuit isn't mounted,then PC4500 and PC4501 aren't also mounted.



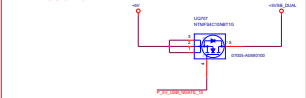
REF	DEF	MODE	INITIAL	UNIT	VALUE	UNIT
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1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1



<Unlabeled Revision>

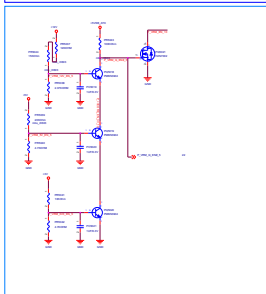
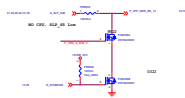
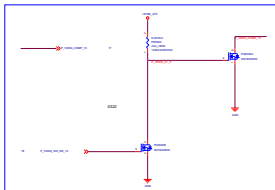
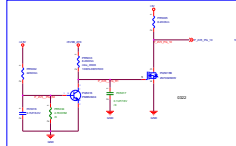
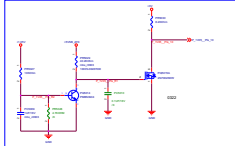
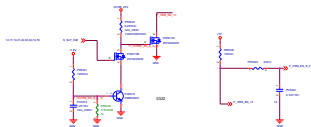


### DPAK MOS 9 mohm



### DPAK MOS 9 mohm





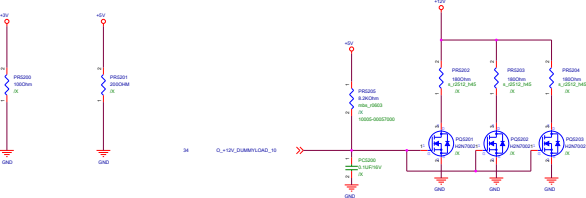


- 1. Vin and Vout keep more than 10mV away
- 2. Input sig and Output signal? use same QND.
- 3. P\_IV\_GATE\_30 is away from Vin more than 10mV ,from Vout more than 10mV.
- 4. If use +3V\_OVP sch, PCB 100 & PCB101 part number change to 11304-02 10P000

Whether to use +3V\_OVP sch, please confirm with EE.

Product Name:

		Title : +3V_OVP	
Additional Comments:		Engineer:	
Date:	Prepared by:	Rev:	
1/21	FME PLUS	1/00	
Drawn: 100-10-00000		Checked:	100-10-00000

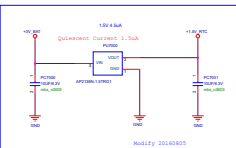


<Variant Name>

<b>ASUS</b>		<b>Title :</b>	
ASUSTek Computer Inc.		<b>Engineer:</b>	
Size	Project Name	Rev	
A3			
Doc	Friday, May 18, 2018	2018	110

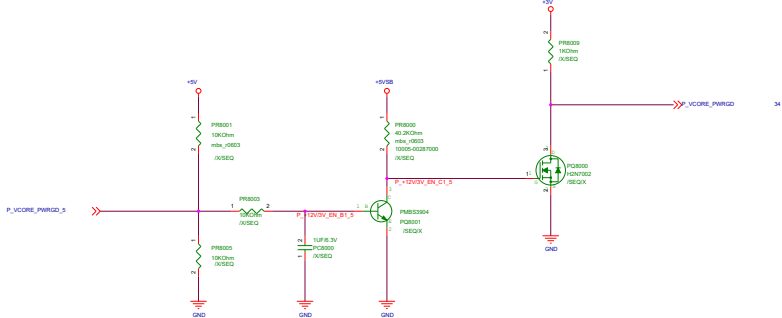


# FAST DISCHARGING



<Standard Name>

		Title : +1.5V_RTC	
ASUSTek Computer Inc.		Engineer:	
Date	Project Name		Rev
A0	AM4		1.00



<Variant Name>

		<b>Title :</b> VCore PWRGD Glitch	
ASUSTek Computer Inc.		<b>Engineer:</b>	
Size A4	Project Name <b>AM4</b>		Rev 1.00
Date Friday, May 18, 2018	Sheet 28	of 115	

<Variant Name>

Title

<Title>

Size

A

Document Number

<Doc>

Rev

<RevCode>

Date:

Friday, May 18, 2018

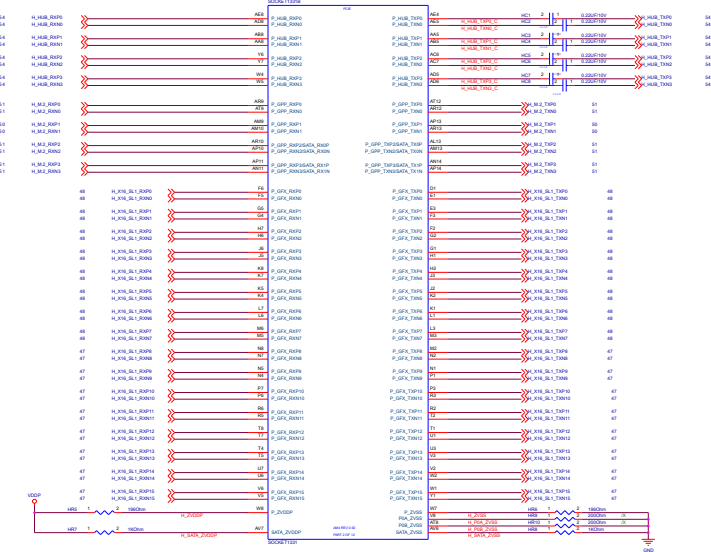
Sheet

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of

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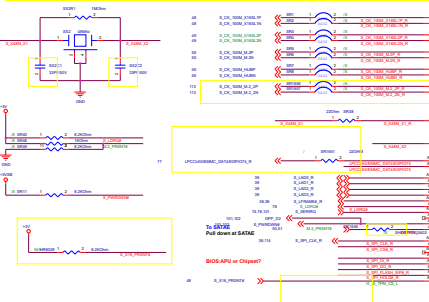




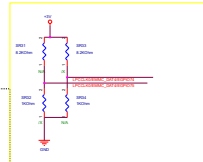
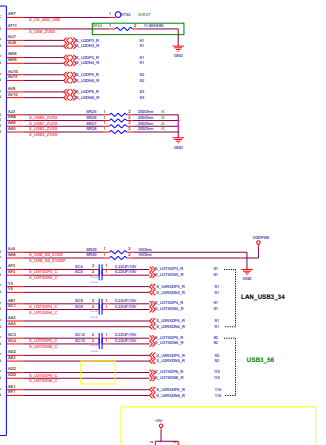
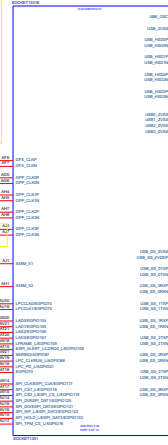
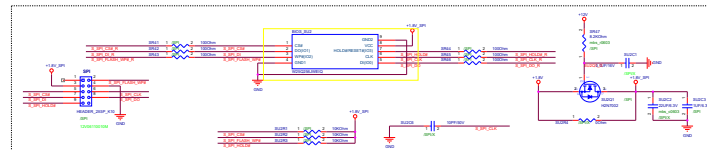
<Variant Name>

		Title : AM4-02	
		Engineer: ElaineX_Li	
Drawn	Project Name	Rev	
A3	AM4	0.01	
Date: Friday, May 16, 2014		Drawn	By: Li





Connect LPC clock 1 to LPC devices that are powered in S0.  
Connect LPC clock 0 to LPC devices that are powered in S5 only if the integrated microcontroller (IMC) is enabled.



<Variant Name>

Title

<Title>

Size

A

Document Number

<Doc>

Rev

<RevCode>

Date:

Friday, May 18, 2018

Sheet

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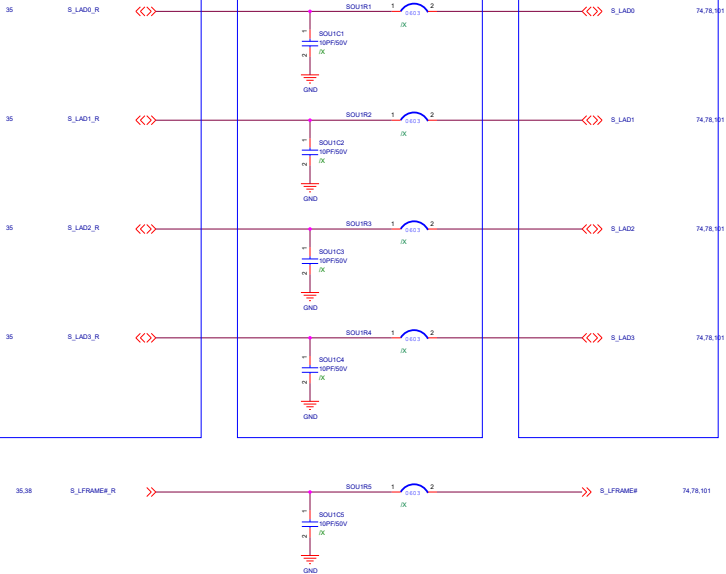
of

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APU SIDE

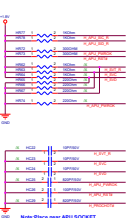
Place near SIO

SIO SIDE

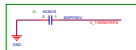


&lt;Variant Name&gt;

<b>ASUS</b>		Title : <b>AM4-09</b>	
ASUSTek Computer Inc.		Engineer: <b>ElaineX_Li</b>	
Size A4	Project Name <b>AM4</b>		Rev 0.01
Date: Friday, May 18, 2018	Sheet 30 of 115		

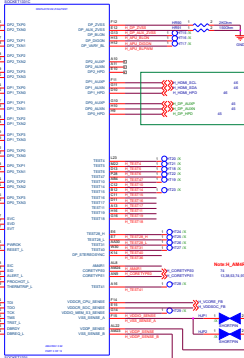


Note:Place near APU SOCKET



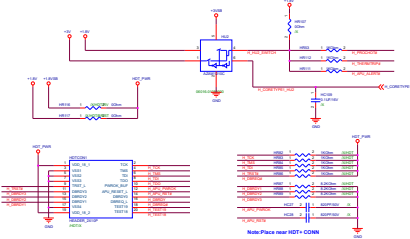
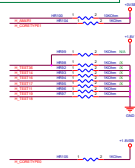
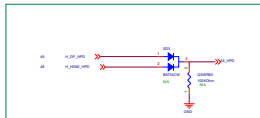
Note:VR113 Place near VIM controller

Note:PROCHOT, THERMTRIP, ALERT# read check  
Note:PROCHOT, THERMTRIP, ALERT# pull high  
Type1: +5V  
Level:4.0V  
Type2: 3.3V  
Type3: No



Note: H\_AMSR1 control APU power on as sequence

Note:Need Check which power should be sense.

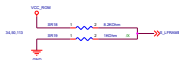
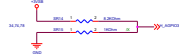
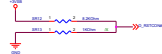


Note:Place near HDT+ CONN

CORETYPE1	CORETYPE0	Family/Model No.	AM4 Type
0	0	F15hM00h-0fh	Type0 Bristol
0	1	Reserved	Type1 ZP
1	0	F17hM00h-0fh	Type2 Summit
1	1	F17hM10h-1fh	Type3 Raven

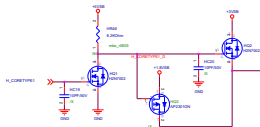
TS1#Level shift

ASUS Title: AM4-03  
Engineer: Wanwei\_Li  
AM4  
Date: 2017.05.10



	TYPE0 2	TYPE0	TYPE0	TYPE0	TYPE0	TYPE2 3
PIN	LFRAME_L	LPCLCLK1	LPCLCLK0	RTCCLK	SYS_RESET_L	AGPIO3
NET	S_LFRAME#_R	S_CK_33M_SIO	S_CK_33M_LPC	S_RTCCLK	O_RSTCON#	H_AGPIO3
PULL HIGH	SPI ROM Default	48M source and generate both internal and external clocks Default	Boot Fail Timer Enable	Coin Battery is onboard Default	Normal Reset Mode Default	Enhanced Reset Logic For Fast Resume From S5 Default
PULL LOW	LPC ROM	100M source and generate internal clock only	Boot Fail Timer Disable Default	Coin Battery is not onboard	Short Reset Mode	Traditional Reset Logic
						SPI_CLK (ZP)
						S_SPI_CLK

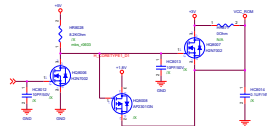
CORETYPE1	CORETYPE0	Family/Model No.	AM4 Type	
0	0	F15hM00h-6Fh	Type0	Bristol
0	1	Reserved	Type1	ZP
1	0	F17hM00h-6Fh	Type2	Summit
1	1	F17hM10h-1Fh	Type3	Raven



10.30.63.76.87

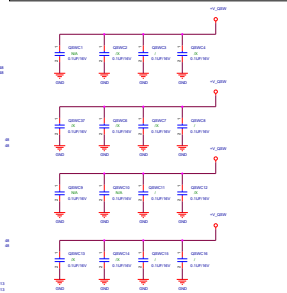
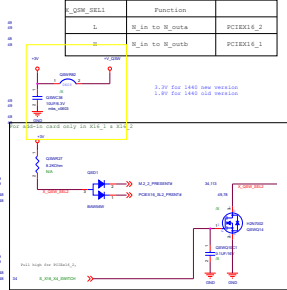
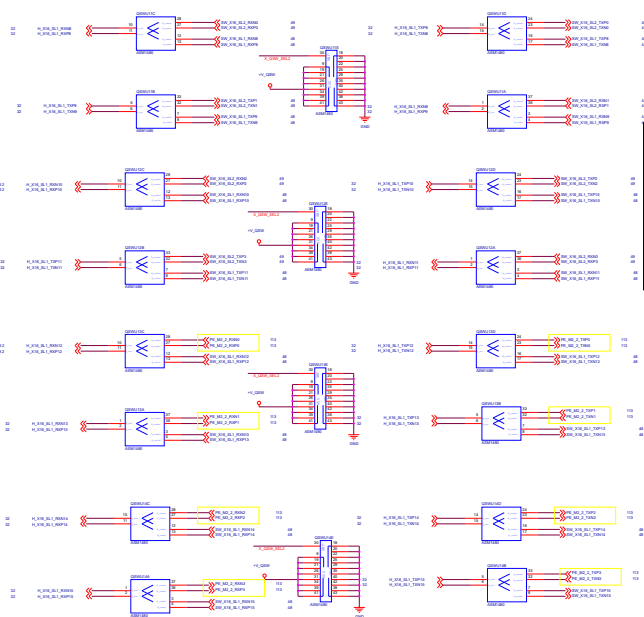
H\_CORETYPE1

APU TYPE	H_CORETYPE1	VCC_RTC
Type0	0	+3VSB
Type2,3	1	+1.8VSB



<Default Name>

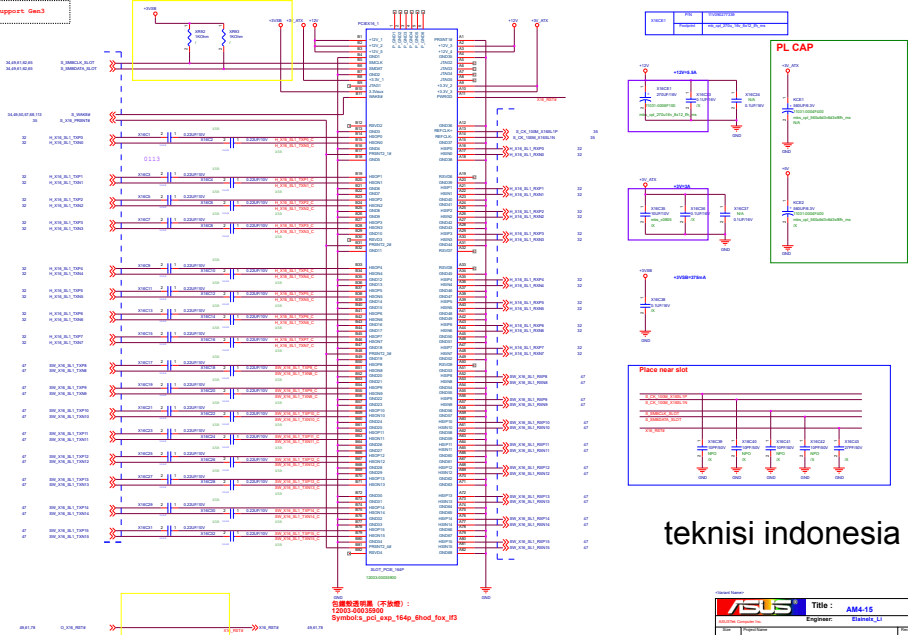


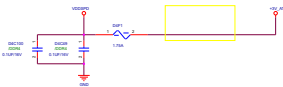


<Default Name>

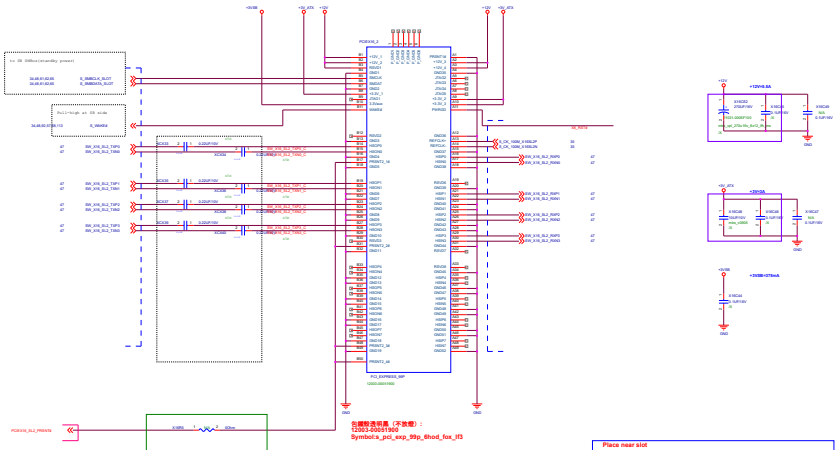




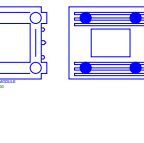
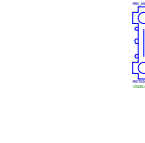
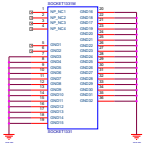
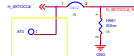




Support Gm3



Downloaded

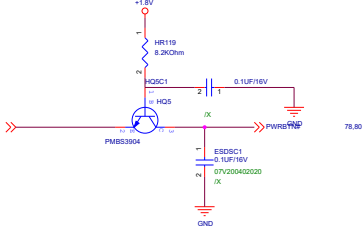


Version: 1.0

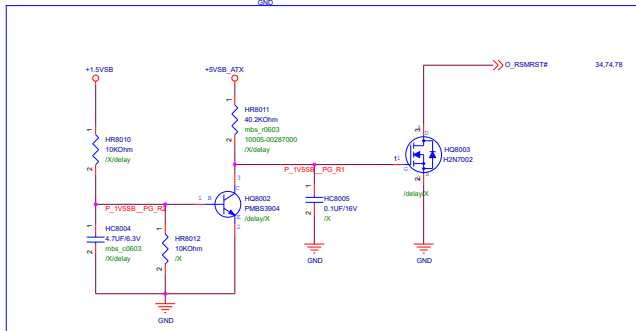


5,33

H\_THERMTRIP#



78,80



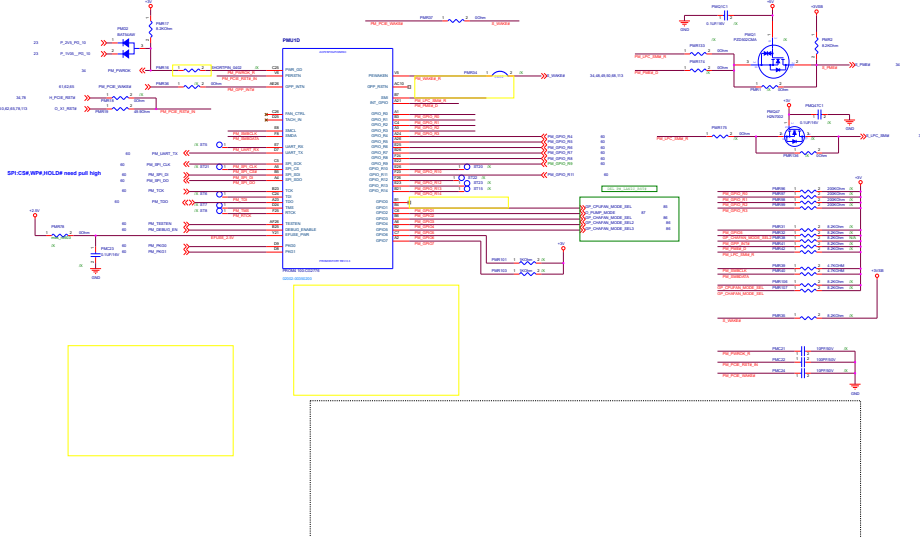
&lt;Variant Name&gt;

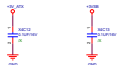
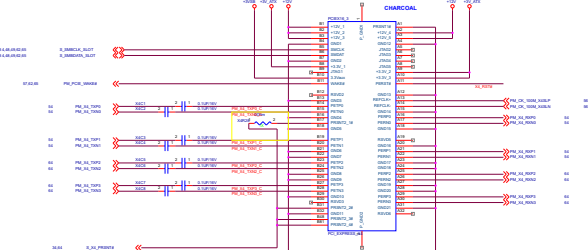
Title			
<Title>			
Size	Document Number		
A	<Doc>		
Date:	Friday, May 18, 2018	Sheet	52 of 115
			Rev
			<RevCode>



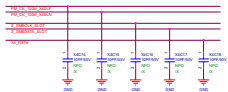








#### Place near slot



From  
SIO

48.00.78



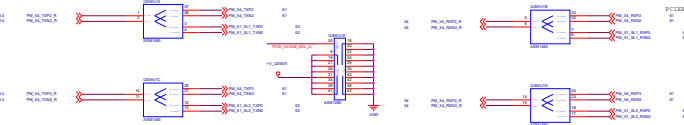
©2007 Starline





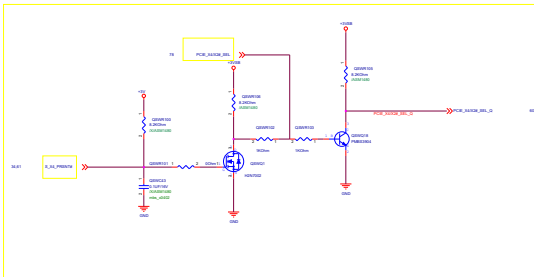
<Default Screen>

		<b>Title :</b> PROM-09	
ASUS Inc. Computer Inc.		<b>Engineer:</b> Elainah_LJ	
Name: AD	Original Version: AM4	Rev: 0.01	Date: 2020 May 18, 2020
Page: 01	Total: 01	of: 01	of: 01

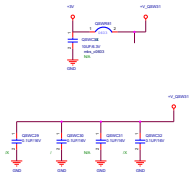


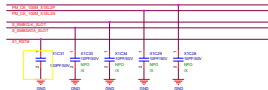
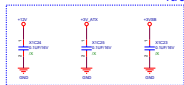
PCIE_X#_SEL	Function	
L	H_in to H_outa	PCIE_X4
H	H_in to H_outb	PCIE_X2/PCIE_X1*2

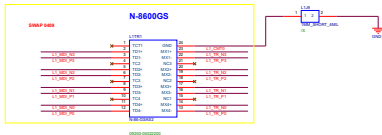
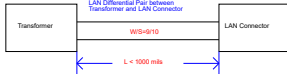
BIOS chose by PCIE\_PGNT#



3.3V for 1440 new version  
1.8V for 1440 old version



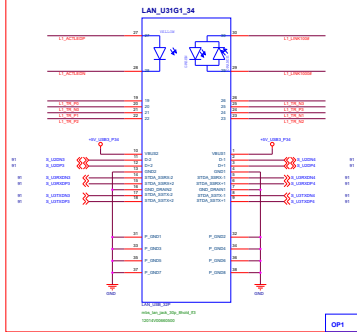




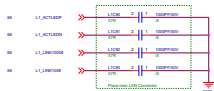
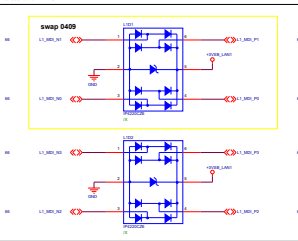
# OP1 - Connector

## GLAN + USB3 \*2 Connector without Transformer

single LAN named LAN\_USB3\_xx  
dual LAN named LAN1\_USB3\_xx



Delete it for EMS



©2014-2015 Taiwan

## LAN1 POWER

1. LAN IC power change to +3VSB\_ATX (remove short-pin L1R88, add resistor L1R88 & L1R89)

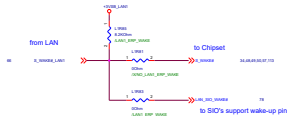


## for Intel PHY

2. for Intel PHY LAN, L1\_LAN\_DISABLE# renamed L1\_LAN\_DISABLE#\_R in LAN IC Page
3. for Intel PHY LAN, L1\_LAN\_DISABLE# pull high resistor L1R7 Optional change to /LAN1\_ERP\_WAKE
4. for Intel PHY LAN, L1\_LAN\_WAKE# renamed L1\_LAN\_WAKE#\_R in LAN IC Page

## for PCIE LAN1

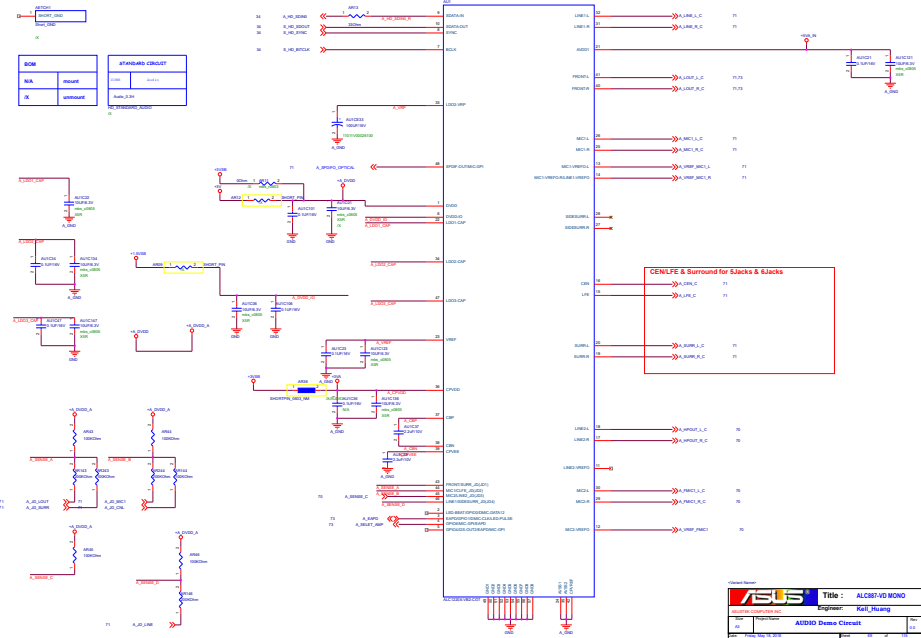
5. for Intel PCIE LAN, L1\_DEV\_OFF# choose +3VSB\_ATX power plane GPIO
6. for PCIE LAN, S\_WAKE# renamed S\_WAKE#\_LAN1 in LAN IC Page



\*Owner's Name

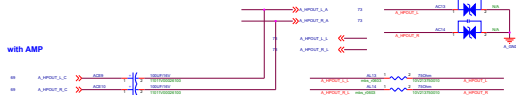
<b>ASUS</b>		Title : Deep S4/S5 Wake	
ASUSTeK COMPUTER INC.		Engineer: Keli_Huang	
Project Name	LAN Demo Circuit	Rev	1.0
Rev	1.0	Rev	1.0
Date: 2018.05.16		Rev	





# for ALC887-VD2/ALC892/ALC1150

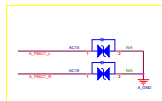
with AMP



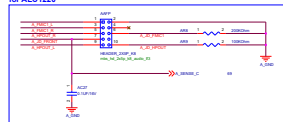
DIP CAP  
 AC 1000 : 118040810743  
 PL 10000 : 110317000019000  
 Audio 10000 : 11011-0002 6000  
 Game 10000 : 11011-0002 9000

AL13, AL14  
 75 Ohm: 10W213750010  
 47 Ohm: 10W211470010

# for ALC891



for ALC1220



Delete it for EMS

		<b>Title :</b> AAFP	
ASUS COMPUTER INC.		<b>Engineer:</b> KeR_Huang	
Project Name:		AUDIO Demo Circuit	
Date:	File Path:	Size:	Version:

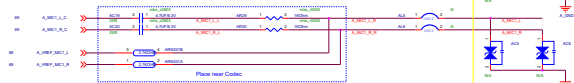
## with AMP/De-POP



## Capless, only for ALC891



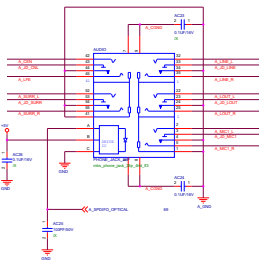
for Gamer Project, Line in use 10UF DIP CAP ACE11, ACE12



Place near Codec

## SMD CAP

DIP CAP  
 RL 100 : 110040822620  
 PL 100 : 11W90106207  
 Audio 100 : 11011-00040600  
 Gamer 100 : 11011-00040600  
 RL 1000 : 110040810743  
 PL 1000 : 110311V0001P000  
 Audio 1000 : 11011-00024000  
 Gamer 1000 : 11011-00024000

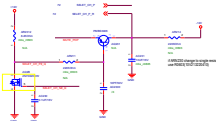
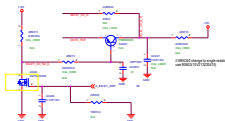


\*Default Status

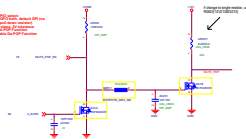


SELECT AMP	MOS A/B	MOS C
Low	On	Off
High	Off	On

MOS	AMP with Switch	No Switch (iAMP with No PNP)
AMP SWITCH	Insert	Remove
AMP NO SWITCH	Remove	Insert

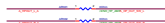
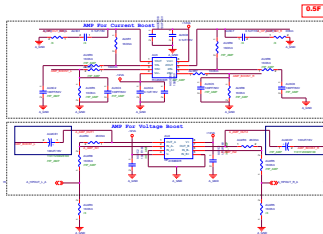
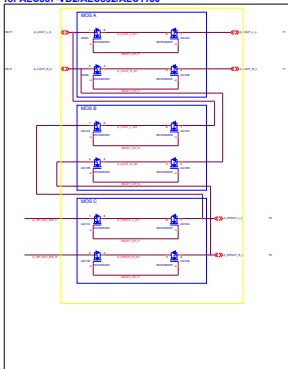


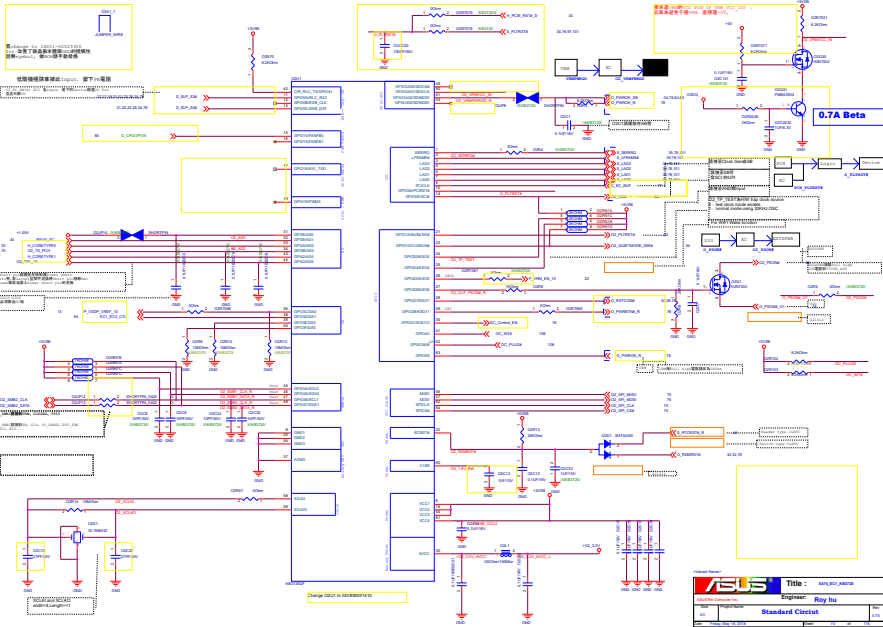
NOTE: PNP AMP (PNP) driver  
1. Select the PNP (PNP) driver  
2. Select the PNP (PNP) driver  
3. Select the PNP (PNP) driver  
4. Select the PNP (PNP) driver



AMP	SWITCH
Active Switch ON	Low
Active Switch OFF	High

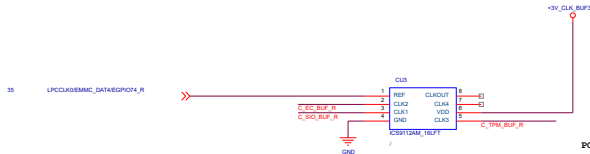
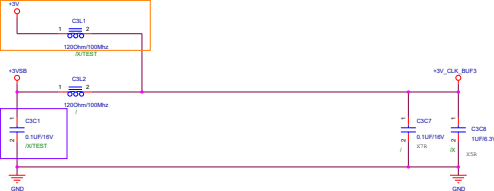
for ALC887-VD2/ALC892/ALC1150











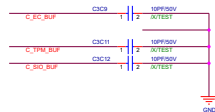
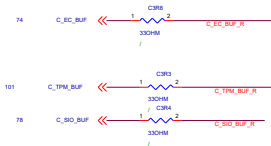
Function Table

Input		Output
G	CLK	Y (0:4)
L	X	L
H	H	H

X: High  
L: Low  
H: Don't care

PCI 24MHz

CLOCK Output



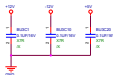
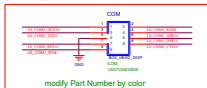
PB277-V DELUXE R1.00



## COM Circuit

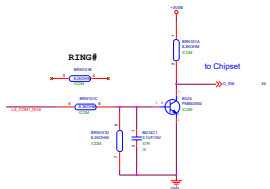
1. Choose COM Port Connector/Header Type
2. Modify O\_R# pill-high by Project
3. For 84 Pin SIO, choose use R# to do Deep S4/S5 wake-up by Project

### COM Box Header

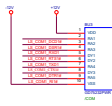


## COM PORT

COM	need COM Port	no COM Port
COM	mount	unmount
JK	unmount	unmount



### Normal

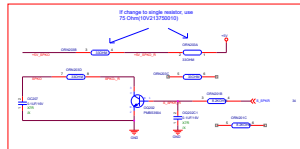
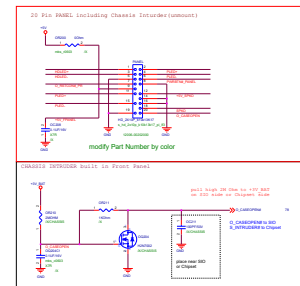
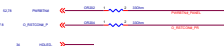
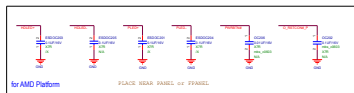


LAN Deep S4/S5 wake-up	COM Port	Q1R171	Q1Q171
support	mount	unmount	mount
not support	mount	mount	unmount
support	unmount	unmount	unmount
not support	unmount	unmount	unmount

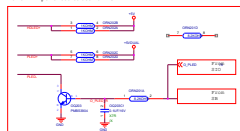
©2009 ASUS

# Panel Circuit

1. Choose PANEL/F\_PANEL Circuit + Chassis Intruder by Project
2. Choose Chassis Intruder Signal connect to SIO or Chipset by Project
3. If mount Chassis Intruder, modify /X/CHASSIS to /CHASSIS
4. Choose SPEAKER Header Circuit + BUZZER Circuit by Project
5. If SPEAKER Header & BUZZER co-lay, the Optional of SPEAKER change to /SPEAKER\_4PIN
6. Choose PLED Circuit by Project
7. Choose PLED control by SIO or Chipset
8. If use Memory Power control PLED, check Memory Power Net Name is correct or not
9. Choose Stand By LED Circuit by Project
10. Check and modify the Optional of Stand By LED Circuit to meet Project requirement



Power LED power source use +5VDDUAL

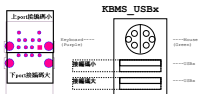
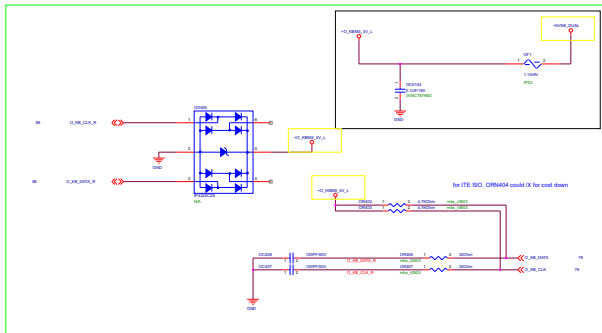


0. PLED\_PLED\_PLED signal  
1. Signal with same frequency, output (SPK) internal pull down resistor) or (SPK high)  
2. Signal to power plane, 10V tolerance  
3. SPK or PLED signal to turn on Power LED  
4. Switch control

Project Name



1. Choose KBMS Port Connector by Project
2. Choose KBMS Power Source by Project
3. If KBMS share power with USB Port, modify Share Power Net Name by Project
4. If choose KBMS Connector, KBMS Signal to-GND Cap choose Single Capacitor or RES Cap by Project
5. If choose KB & USB 2.0 Connector, check USB 2.0 Port D+/D- Signal begin with 0 or 1, then modify USB 2.0 Port D+/D- Signal Net Name by Project
6. If choose KB & USB 3.0 Connector, modify USB Port TX/RX/D+/D- Signal Net Name by Project
7. If choose KB & USB Connector, modify USB Port Power Net Name by Project
8. If choose KB & USB Connector, modify Connector Port Reference by Project
9. If choose KB & USB Connector, for ITE SIO, ORN404 could /X for cost down

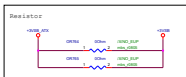


## ERP Circuit

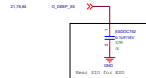
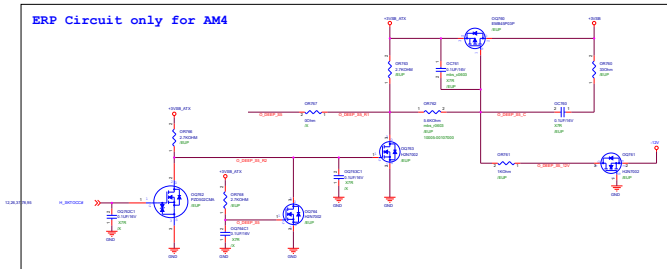
### 1. Choose ERP Circuit by Project

BOM	no SIO ERP & SIO DSW	SIO ERP	SIO DSW
NO_EUP	mount	unmount	unmount
EUP	unmount	mount	mount
NO_SIODSW	mount	mount	unmount
SIODSW	unmount	unmount	mount

### ERP Circuit



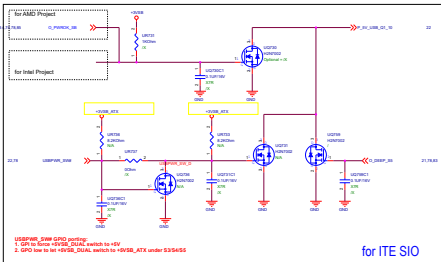
### ERP Circuit only for AM4



# USBPWR\_SW# Circuit for ITE SIO

1. Choose USBPWR\_SW# Circuit by Project
2. Check PWROK Signal Net Name by Platform
3. For AMD AM4 Project, UR733 & UR736 pull-high power change to +3VSB

+5VSB\_DUAL default no power, reserve USB Inrush Circuit



<Variant Name>

		Title : USB Power Control	
ASUSTeK COMPUTER INC.		Engineer: Kai Huang	
Doc	Project Name	Super I/O Demo Circuit	
Content			
Rev	Rev	Rev	Rev
Date: Friday, May 18, 2018		Drawn: B4	all: 10.0

3. Choose ☐ PWROK or ☐ PWROK SB by Platform for FAN Expert 3 Mode

GP\_CUFAN\_MODE\_SEL GPIO select:  
 1. could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor must)  
 2. main power plane, 3V tolerance  
 3. GPI to choose Auto-detection Mode operating  
 4. GPO high to force PWM Mode operating  
 5. GPO low to force DC Mode operating



		<b>Title :</b> CPU_FAN	
<b>ASUSTEK COMPUTER INC</b>		<b>Engineer:</b> Kell_Huang	
<b>Date</b> 02	<b>Project Name</b> Super I/O Demo Circuit	<b>Rev</b> 0.0	
Date: Friday, May 16, 2014		Sheet: 20	of: 115

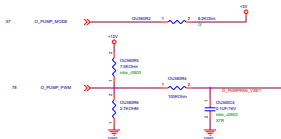
# AIO\_PUMP & W\_PUMP+ Circuit use Single Resistor

1. Choose O\_PUMP\_FT1\_DET Circuit by Project

2. Choose AIO\_PUMP/W\_PUMP+ Circuit by Project

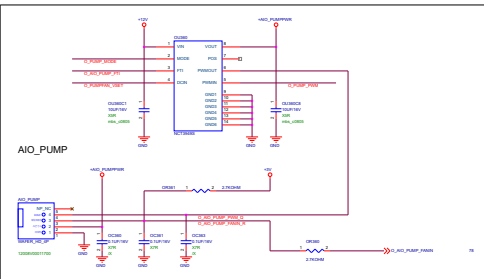
O\_PUMP\_MODE GPIO select:

1. could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor must)
2. main power plane, 3V tolerance
3. GPI to choose Auto-detection Mode operating
4. GPO high to force PWM Mode operating
5. GPO low to force DC Mode operating



GP\_PUMP\_EQM\_ENM GPIO select:

1. could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor must)
2. main power plane or stand by power plane, 3V tolerance
3. GPI to not enter Extreme Quiet Mode
4. GPO low to enter Extreme Quiet Mode



O\_PUMP\_FT1\_DET GPIO select:

1. could be GPI, default GPI (no internal pull-down/pull-high resistor must)
2. main power plane or stand by power plane, 3V tolerance
3. GPI high means 4 Pin FAN
4. GPI low means 3 Pin FAN

Only AIO\_PUMP

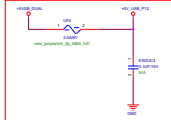
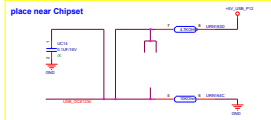


©2020 ASUS

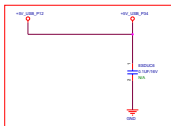
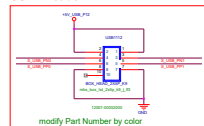
<b>ASUS</b>		Title : PUMP_FAN	
ASUSTeK COMPUTER INC.		Engineer: Kail_Huang	
Rev: 1.0		Super I/O Demo Circuit	
Date: 2020-05-18-2020		Rev: 1.0	



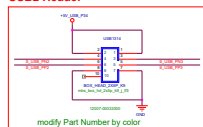
# place near Chipset



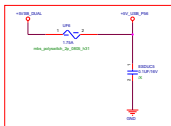
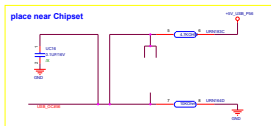
# USB2 Header



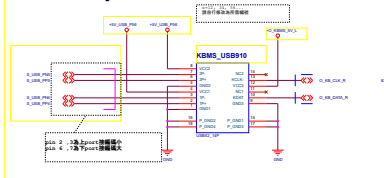
# USB2 Header



# place near Chipset

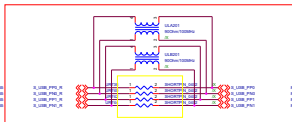
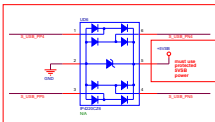
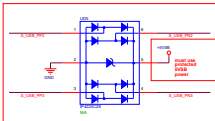
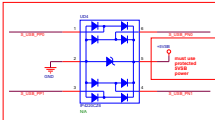


# KBMS+2 port USB2.0

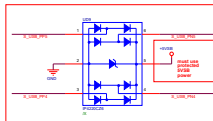
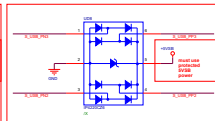
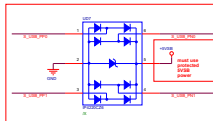
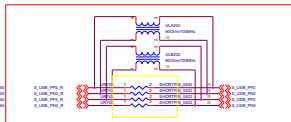
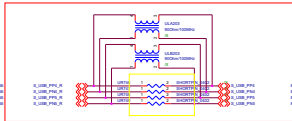


©2008 Starkey

## Reserve Location (RES A)



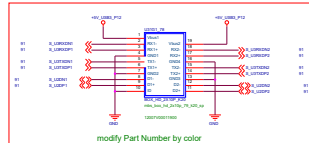
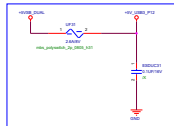
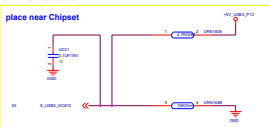
## Reserve EMI Choke (Single RES)



©2014-2015

# OC# circuit for AMD

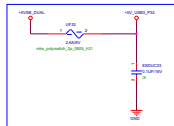
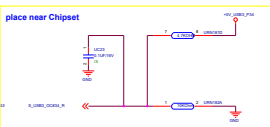
place near Chipset



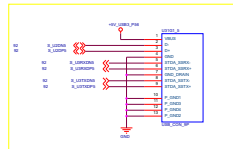
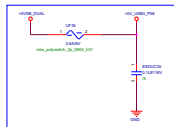
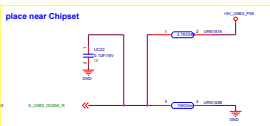
place near Chipset



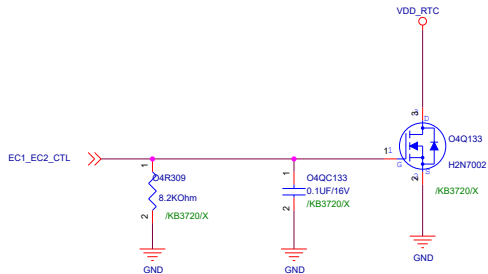
place near Chipset



place near Chipset

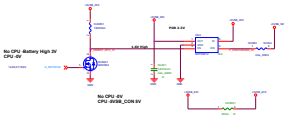


©2007 ASUS



&lt;Variant Name&gt;

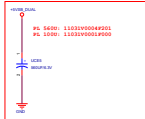
Title		
<Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date:	Friday, May 18, 2018	Sheet 94 of 115



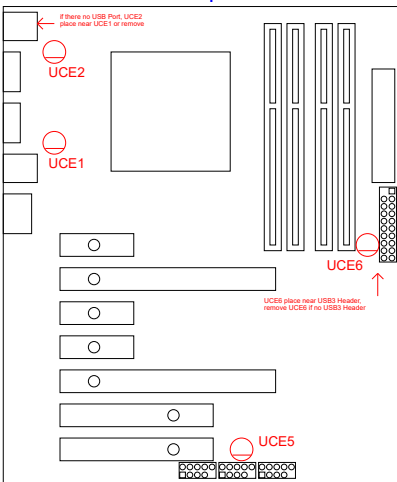
# PL CAP



# PL CAP



# USB Power CAP recommend placement

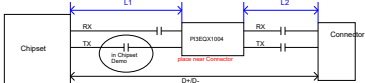


BOM	
N/A	mount
/X	unmount

STANDARD CIRCUIT	
U100	U100
C100, U100	

©2019/2020

ASUS		Title : USB Power CAP	
ASUS PRELIMINARY DESIGN		Engineer: Kai_Huang	
Date		Project Name	
A3		Chipset USB Demo Circuit	
Date		Project Name	
2019, May 28, 2019		Project Name	



Net	Impedance/Width	Space	Length
TX/RX L1	80 - 85 Ohm +/- 10%	30 mils	< 10", prefer 5" - 9"
TX/RX L2	80 - 85 Ohm +/- 10%	30 mils	< 2.5", prefer 0.5" - 1.5"
+3V_RDP2	>= PI3EQX1004 Count *20 mils		
Other Power Net	>= 20 mils		

#### USB 3.1 Re-Driver PI3EQX1004 Circuit

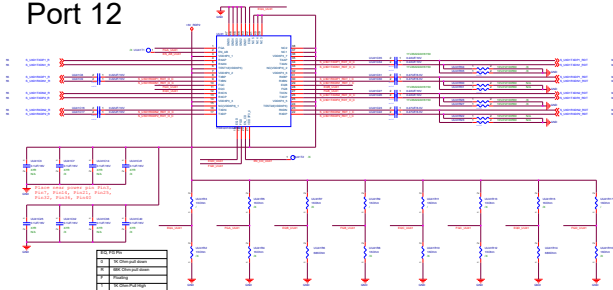
1. Modify USB 3.1 Port TX/RX Signal(input/output) Net Name by Project
2. Choose PI3EQX1004 Power Solution by PI3EQX1004 count
3. When U041 TXA output signals send to ASM1543, U041C34 & U041C35 change from 11V23222416150 to 11G232247415150 & mount U041R04, U041R35
4. When U041 TXB output signals send to ASM1543, U041C26 & U041C27 change from 11V23222416150 to 11G232247415150 & mount U041R06, U041R27
5. When U042 TXA output signals send to ASM1543, U042C34 & U042C35 change from 11V23222416150 to 11G232247415150 & mount U042R04, U042R35
6. When U042 TXB output signals send to ASM1543, U042C26 & U042C27 change from 11V23222416150 to 11G232247415150 & mount U042R06, U042R27
7. When U043 TXA output signals send to ASM1543, U043C34 & U043C35 change from 11V23222416150 to 11G232247415150 & mount U043R04, U043R35
8. When U043 TXB output signals send to ASM1543, U043C26 & U043C27 change from 11V23222416150 to 11G232247415150 & mount U043R06, U043R27

#### Power Solution for PI3EQX1004 \*1

3.3V for PI3EQX1004, 340mA/pcs@80



## Port 12



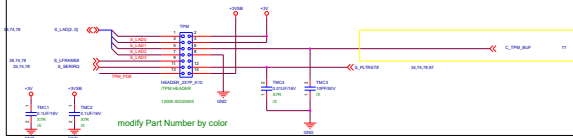
Copyright

[illegible]

can't change  
to nomask



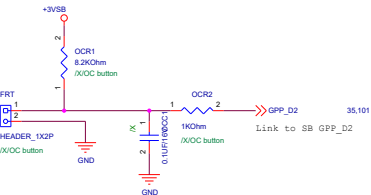
1. Del TPM Header if don't need
2. Del Onboard TPM if don't need
3. Modify TPM Header Clock Net Name by Project
4. Modify Onboard TPM Clock Net Name by Project
5. Modify Onboard TPM IC's Part Number by Project
6. Modify Optional of TMR13, TMR14, TMR15 by Onboard TPM IC



BOM	TPM Header	Onboard TPM
N/A	mount	mount
/X	unmount	unmount
/TPM HEADER	mount	unmount
/TPM IC	unmount	mount

System Name

# OC Button Circuit



<Variant Name>

Title		
<Title>		
Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Friday, May 18, 2018	Sheet 102 of 115



# ASUS PCB Logo

with R

1.5mm without R

2mm without R

2.5mm without R

3mm without R

3.5mm without R

4mm without R

4.5mm without R

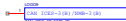
5mm without R

5.5mm without R

6mm without R



PCB MADE IN CHINA



CAN ICES-3 (B)/NMB-3(B)



## ASUS PCB Logo Circuit

1. Choose ASUS Logo by Project
2. Choose CE Logo by Project
3. Keep or remove NEED\_COMP\_SILK by Project



Normal CE Logo



CE Logo for Wifi



# Selling Point

## 1. Selling Point 新增流程及窗口人員



## 2. 如何抓取 Selling Point Part, 如下圖

Search results for "PCB Footprint":

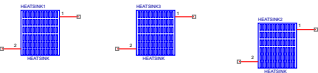
Property	Compare	Value
1	PCB Footprint	Contains: mb_text
2	PCB Footprint	Contains: uefi
3		

Search results for "UEFI BIOS":

Table	Part Number	Component Name	Description	Value	Electric
ASUS_C53	temp_A40000507902	mb_text_uefi_bios	UEFI BIOS		

## 3. Example

定位孔

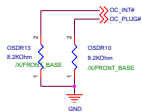


<Variant Name>

<b>ASUS</b>		Title : Fiducial Mask	
ASUSTEK COMPUTER INC		Engineer: Kai_Huang	
Drawn	Project Name	Silkscreen Demo Circuit	
A3			Rev: 0.00
Date	Friday, May 18, 2018	Sheet	105 of 115

Delete it for EMS

ASUS		Title : PCB Impedance Point	
ASUSTEK COMPUTER INC.		Engineer: <u>Keli_Huang</u>	
Project Name	Silkscreen Demo Circuit		
Rev	1.0		
Date	Friday, May 16, 2014		
Page	100 of 100		

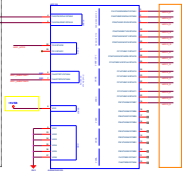
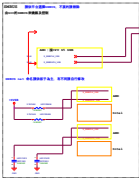


74  
74

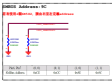
<Variant Name>

		Title :	Cover page
ASUSTek Computer Inc.		Engineer:	Eddie Chiu
Size A4	Project Name Standard Circiut		Rev 1.00G
Date: Friday, May 16, 2015	Sheet	108	of 115

所有使用Addreswmb.Ca線路，需以黃線標記



此處為黃線標記



此處為黃線標記  
此處為黃線標記



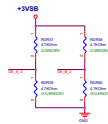






Adjustment for adaptive BQ.  
With JFE 10562

Adjustment for adaptive Kq  
with 100 1000



FME 54 ok

Adjustment for Transmitter out swing.  
With rfd locked

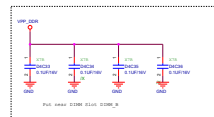
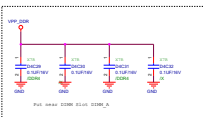
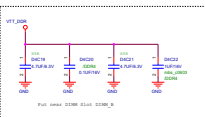
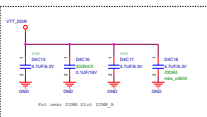
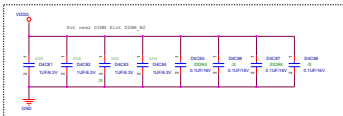
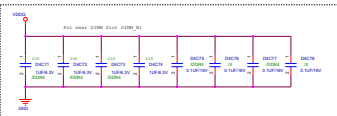
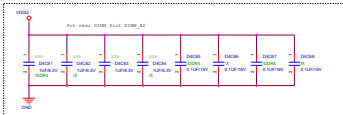
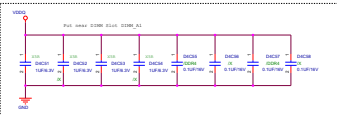
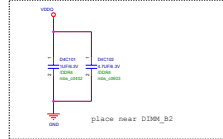
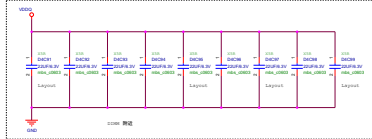
Strapping pin for Channel A/W  
de-emphasis level control.  
100 100ms pull-down

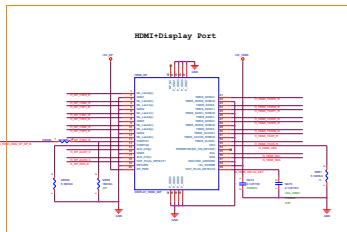
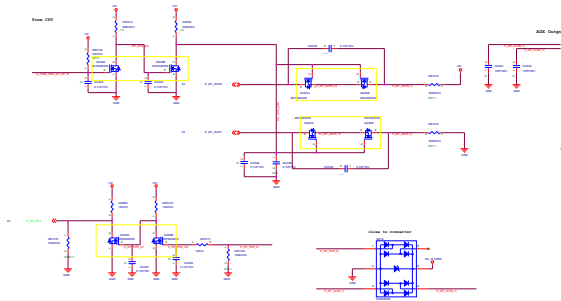
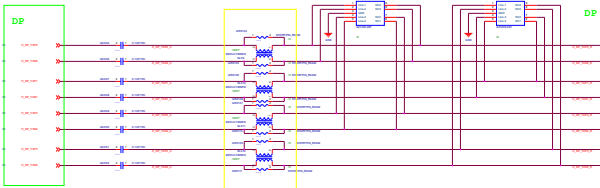
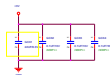
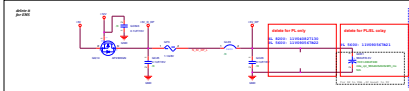
Chip EN disable chip during suspend state for power saving

Only support 3.3V mode I2C signals

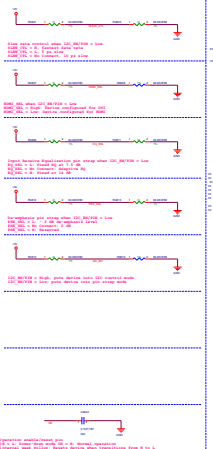


Layout to D403

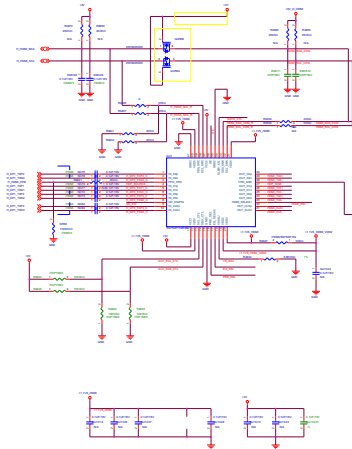
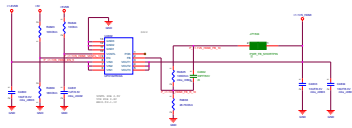




## HDMI Active-Level Shift



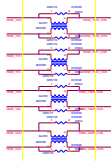
## HDMI LDO 1.1V5



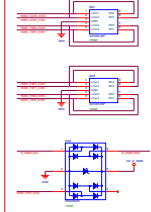
## HDMI PWR\_+5VS\_HDMI



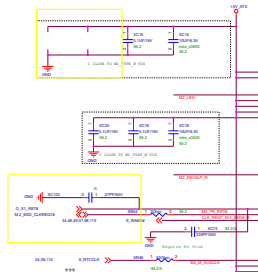
## HDMI EMI



## Del for EMS

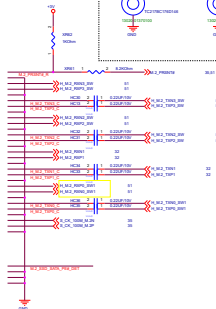
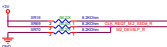


1.740.00.70.102 34



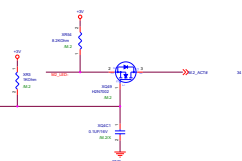
M.2\_100CKMT75  
M2\_100CKMT75

1.740.00.70.102  
M.2\_100CKMT75  
M.2

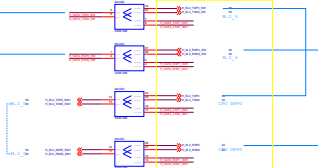
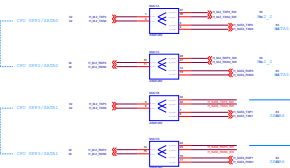


M.2_100CKMT75	
0	M.2 SATA Mode
1	M.2 PCIe Mode

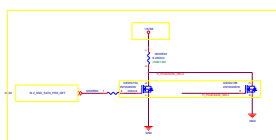
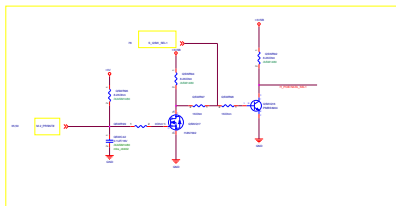
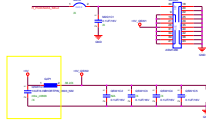
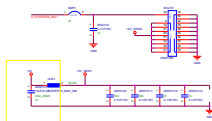
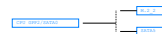
M.2\_100CKMT75



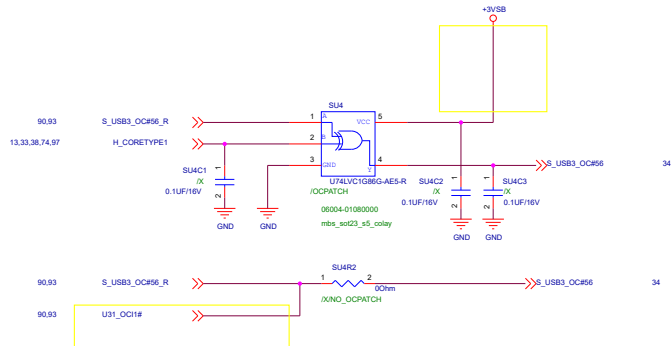
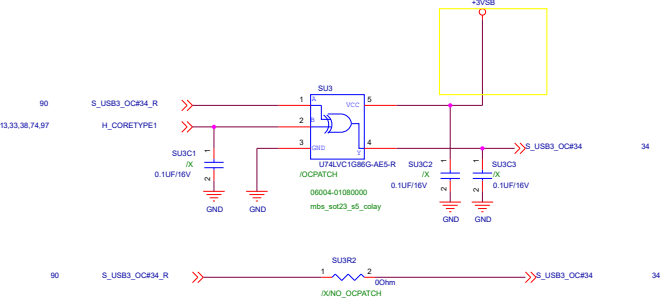
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Pinout List		
L	0, 14 for B_out0	
R	0, 14 for B_out0	



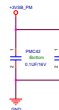
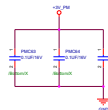
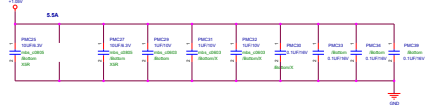




<Variant Name>

<b>ASUS</b>		<b>Title :</b> Patch For USB0C
ASUSTEK COMPUTER INC		<b>Engineer:</b>
Size A4	Project Name	Rev 0.0
Date: Friday, May 18, 2018	Sheet 53 of 115	







```
13071-02420700 ROG STRIX B350-F GAMING TW SE V.S.TECH/T-98TH117-02
|--- 13071-02420400 FCN RS
|--- 13071-02420600 M0GN RS
|--- 13071-02420500 M0GN RS
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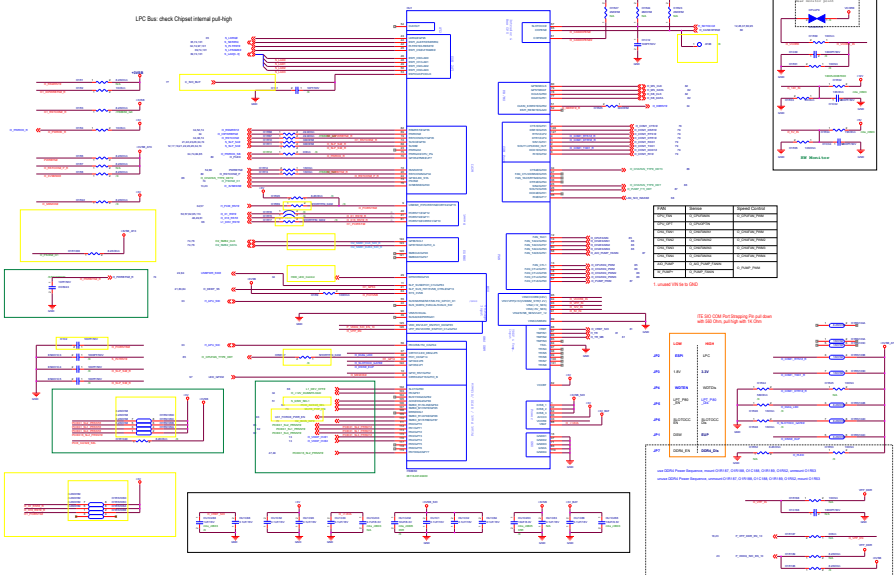


1. Check Pin 51 KBRST# use or not
2. If not use ITB65E DOR4 Power Sequences, modify Optional
3. Del S\_LDRQ# net if unused
4. Del O\_CASEOPEN# off-page if unused

5. Del `AUDIO_LED_PWM` net if unused
6. If add `COM2` Circuit, no `AUDIO_LED_PWM` function
7. Add `BEEP` Signal by Project, choose `GPIO` by mapping table
8. Add `COM` Debug Signal by Project, choose `GPIO` by mapping table

10. Remove unused FANIN/FANOUT signal

LPC Bus: check Chipset internal pull-high



FAN	Source	Speed Control
CPU_FAN	0, CPUFAN0	0, CPUFAN0_Pwm
CPU_OPT	0, CPUOPT0	
CPU_FAN0	0, CPUFAN00	0, CPUFAN0_Pwm
CPU_FAN1	0, CPUFAN01	0, CPUFAN1_Pwm
CPU_FAN2	0, CPUFAN02	0, CPUFAN2_Pwm
CPU_FAN3	0, CPUFAN03	0, CPUFAN3_Pwm
CPU_FAN4	0, CPUFAN04	0, CPUFAN4_Pwm
RAID_FAN0	0, RAID_FAN0_Fan0	0, FAN0_Pwm
RA_FAN0	0, FAN0_Fan0	

1. unused VPI file to CND

ITE SIO COM Port Strapping Pin pull down with 560 Ohm, pull up with 1K Ohm

SCM	
SA	measuri
SE	unmeasuri

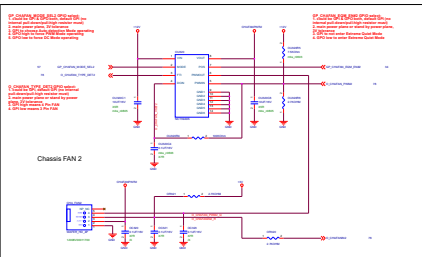
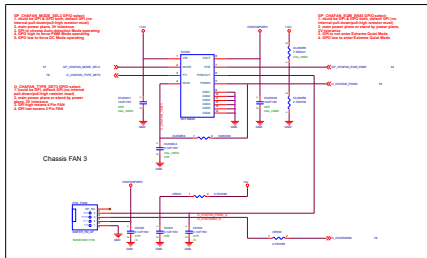
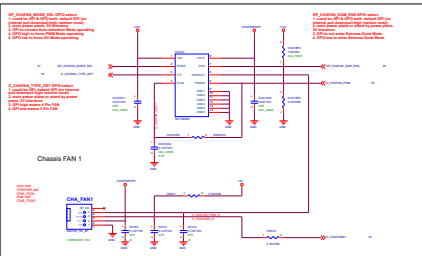
STABILITY CHECK	
TIME	REPORT DATE
TIME (H:MM)	



CHA\_FAN FAN Expert 3 Mode QFAN Circuit use Single Resistor

1. Choose reserve PWM Mode or not by Project
2. Remove the CHA\_FAN which don't need
3. If only one CHA\_FAN, rename CHA\_FAN1 to CHA\_FAN

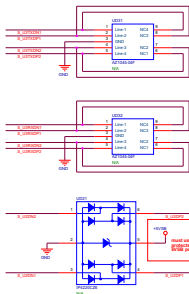
## FAN Expert 3 Mode



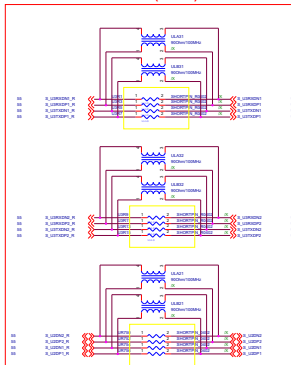
# Port 12

Delete it for  
PART

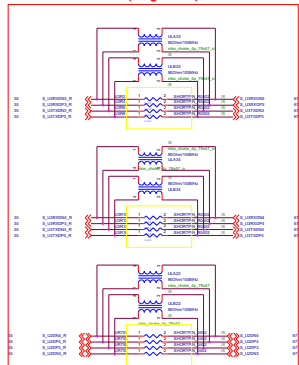
## ESD Diode



## Reserve Location (RES A)

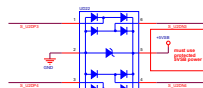
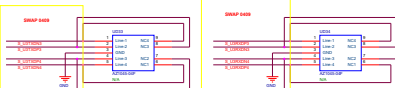


## Reserve Location (Single RES)



Delete it for  
LMS

## ESD Diode

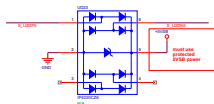


\*Default Status:

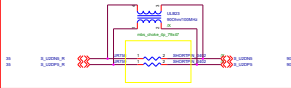
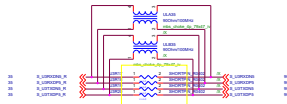
# Port 56

Delete it for  
P56

## ESD Diode



## Reserve Location (Single RES)



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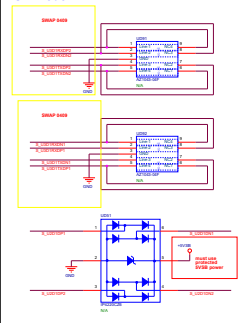




# 3.1 Port 12

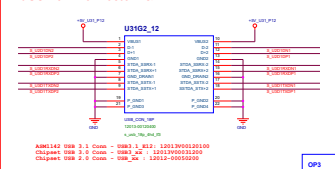
Delete it for  
DMS

## ESD Diode

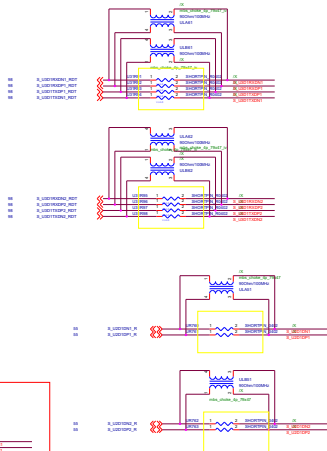


## OPS - Connector

### Ext USB 3.1 Connector 1&2

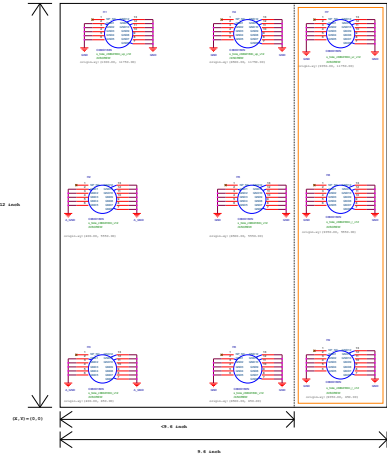


## Reserve Location (Single RES)



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## Screw Hole



Screw Select

	Standard (2.0 x 3.0 x .05)	Standard (2.0 x 3.0 x .05)
M2	✓	✓
M2.5	✓	✓
M3	✓	✓
M3.5	✓	✓
M4	✓	✓
M4.5	✓	✓
M5	✓	✗
M6	✓	✗
M8	✓	✗

M2 SCREW FOOTPRINT

L\_2mm\_1mm0mm0mm\_1mm



L\_2mm\_1mm0mm0mm\_1mm



L\_2mm\_1mm0mm0mm\_1mm



L\_2mm\_1mm0mm0mm\_1mm

Fiducial Mask  
(光學點)

光學點圖樣，一組  
適合不同板型之圖樣大小及版本需求  
適合不同板型之圖樣  
適合不同板型之圖樣  
適合不同板型之圖樣

大顆光學點

小顆光學點

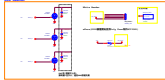
大顆十字光學點

小顆十字光學點



## 4. 外置一體電源的環境

Fig. 1000000





# 4. 外控一般電機的情況

圖 10-10-1



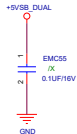
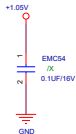
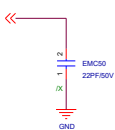
# AUDIO COVER



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<Title>		
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S\_SPI\_CLK\_R



&lt;Variant Name&gt;

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<Title>		
Size	Document Number	Rev
A	<Doc>	<RevCode>
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